Electronics for a Position & Time Sensing Large Area Photo-Detector System

Eric Oberla

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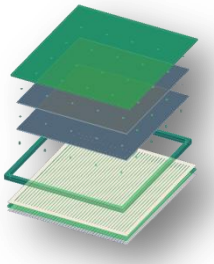
ANT‘11



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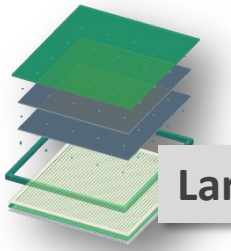
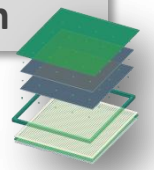


Large-Area Picosecond Photo-Detectors (LAPPD) Collaboration

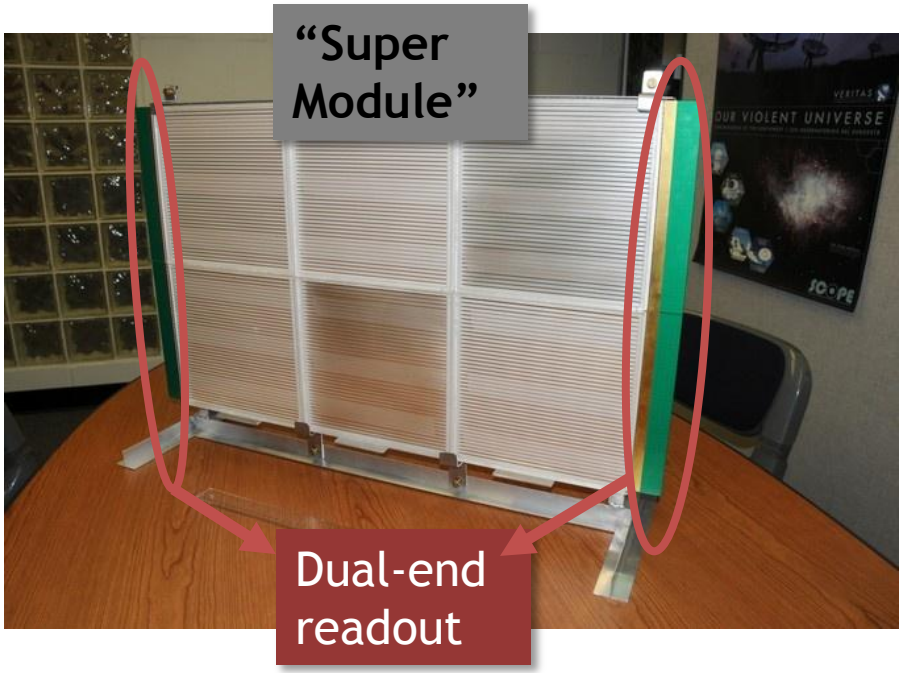


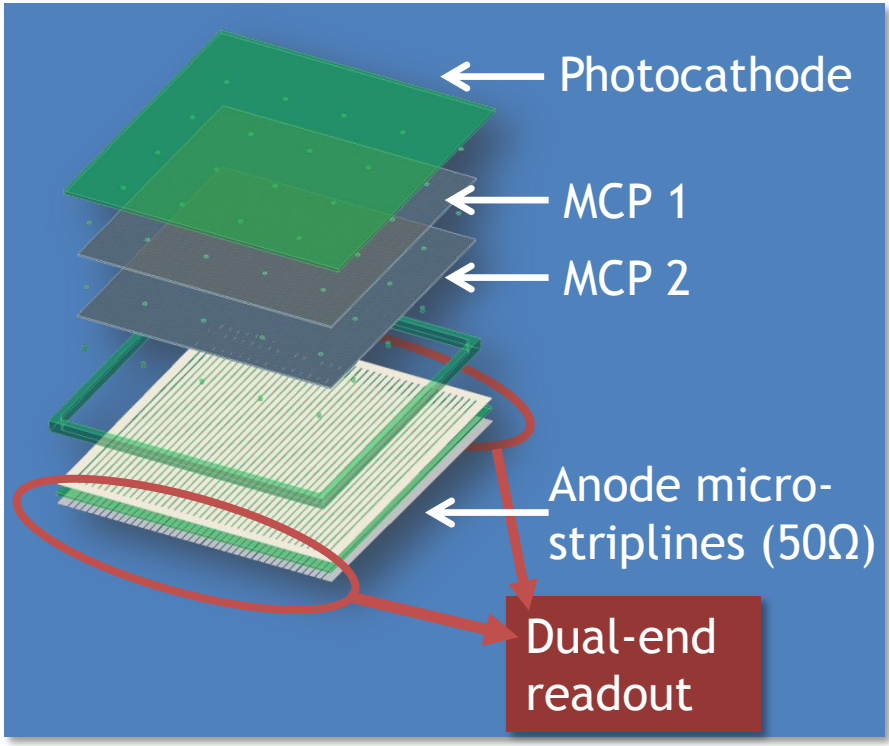
Outline

- **LAPPD Anode**: Transmission line readout
- **Front-end**: Gigahertz waveform digitizing ASICs
- **System**: DAQ development

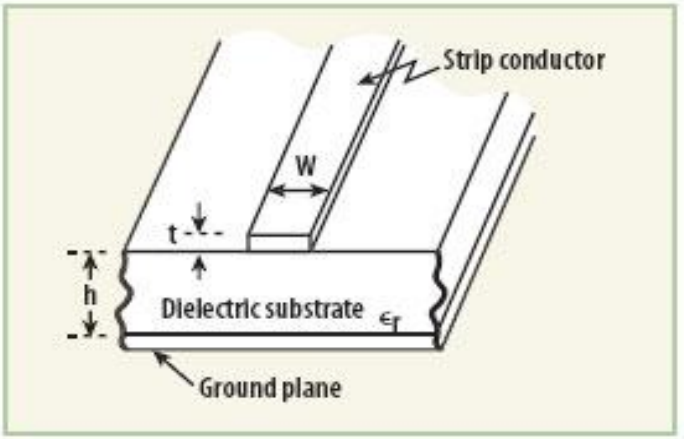
The LAPPD project

- Development of large-area, relatively inexpensive Micro-Channel Plate (MCP) photo-detectors
  - 8” x 8” phototubes = ‘tile’ (large active area)
  - Gain >= 10^6 with two MCP plates
  - Transmission line readout – no pins!
  - Fast pulses + low TTS ~30ps





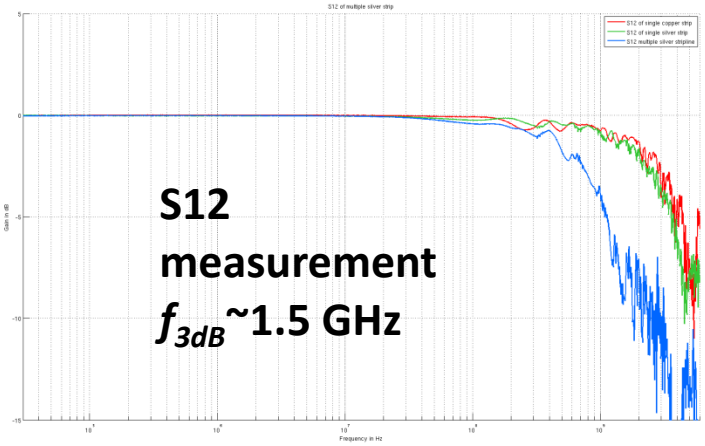
Transmission Line Anode



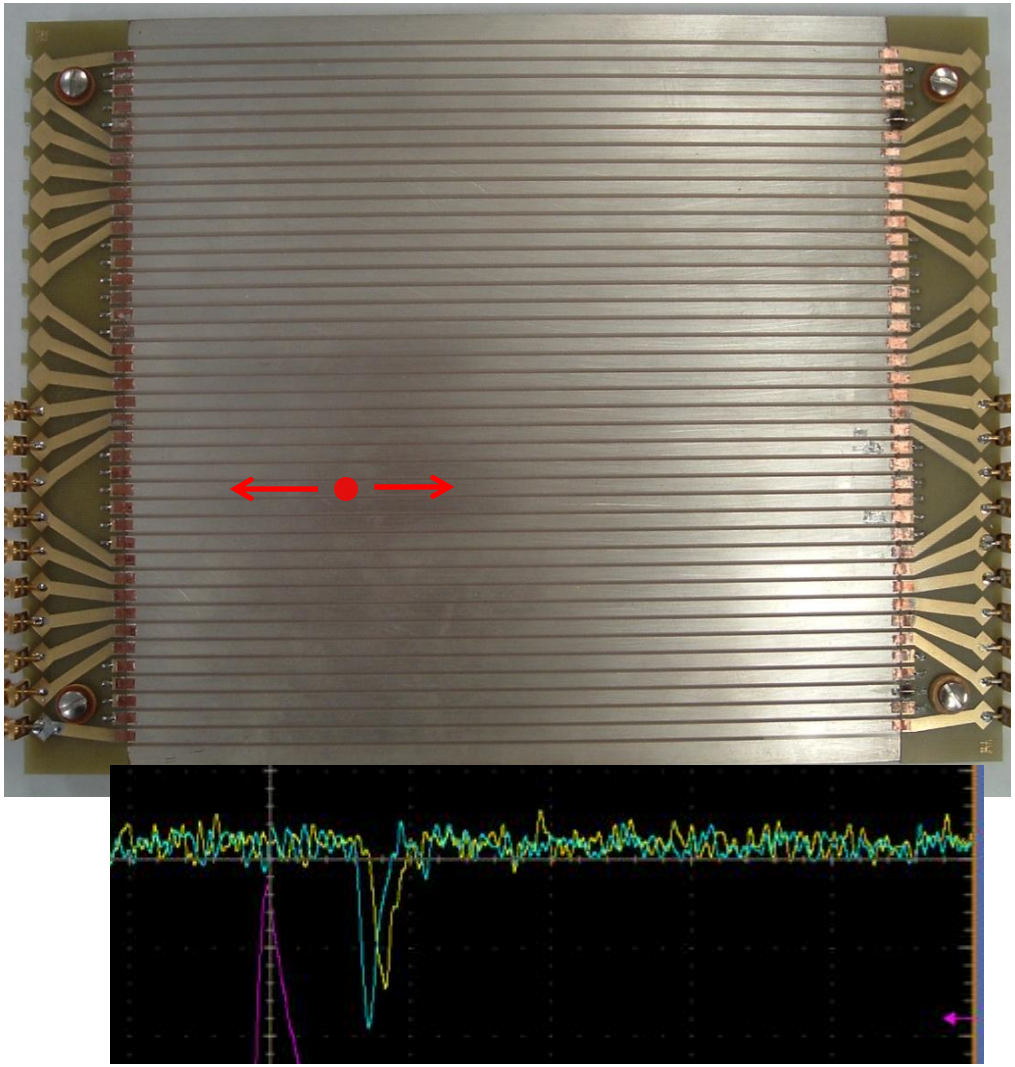
1. Microstrip transmission lines consist of a strip conductor and a ground metal plane separated by a dielectric medium.

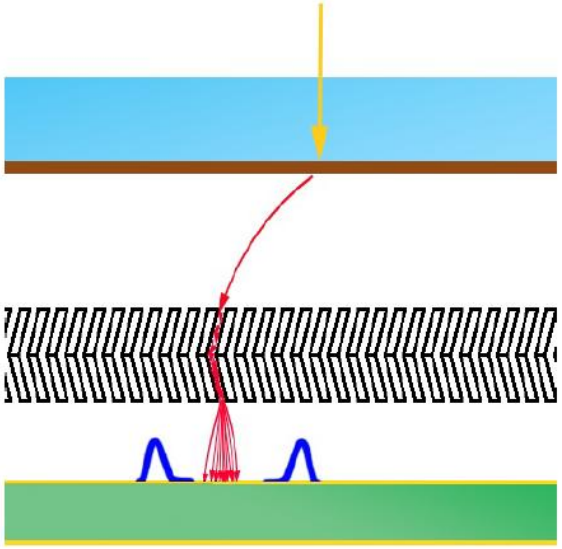
Microwaves & RF

- 30 microstrip transmission lines (Z_o=50Ω)
  - 0.108” thick glass substrate, 0.182” strip width
  - quasi-TEM mode (crosstalk)



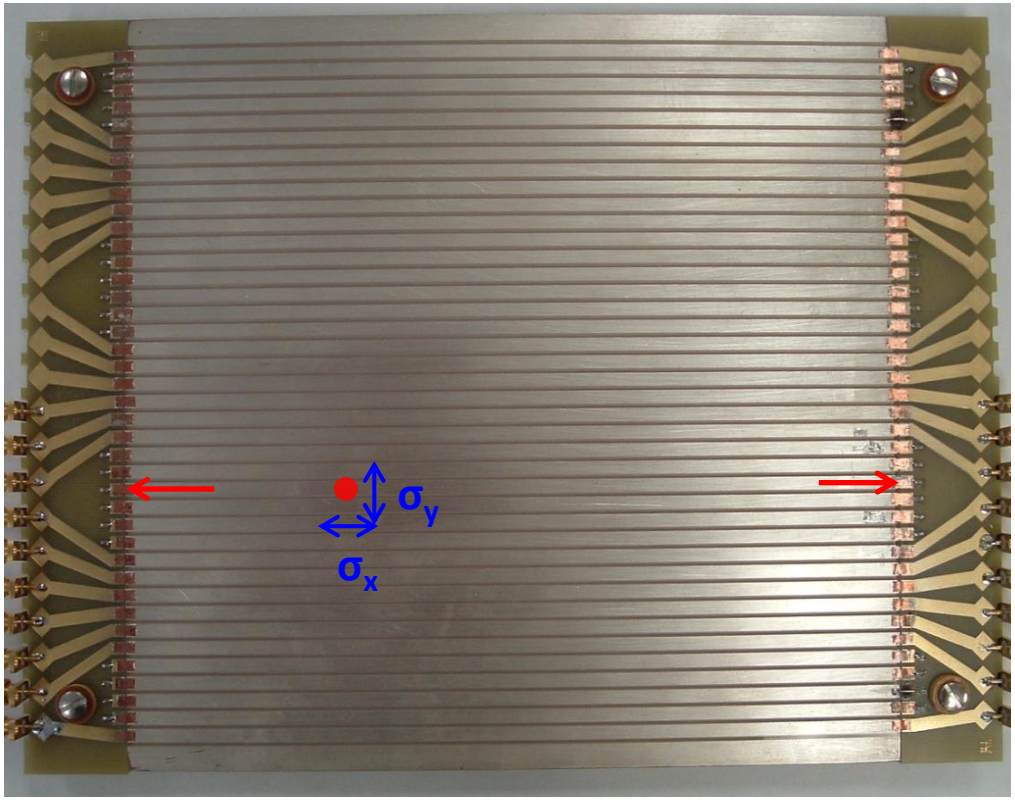
Transmission Line Anode

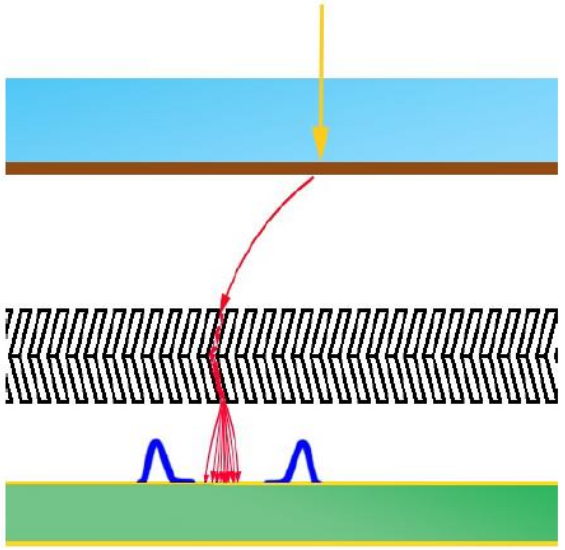




After final amplification, the shower of electrons is accelerated towards the anode, inducing EM waves that propagate in both directions along transmission line.

Transmission Line Anode





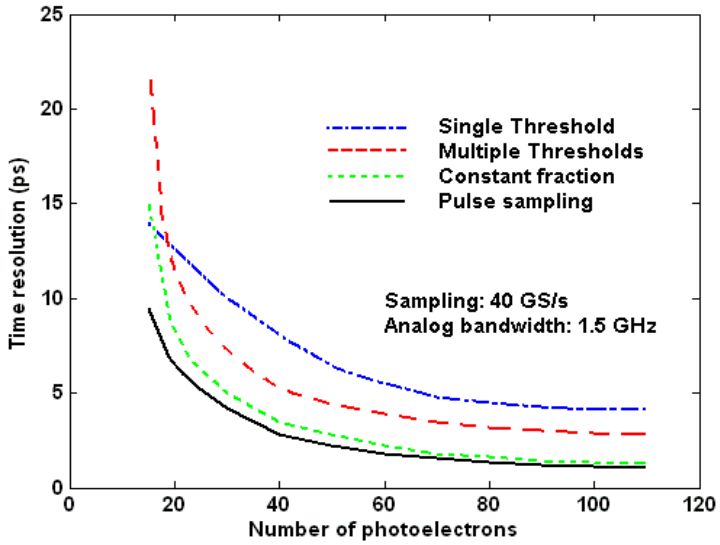
After final amplification, the shower of electrons is accelerated towards the anode, inducing EM waves that propagate in both directions along transmission line.

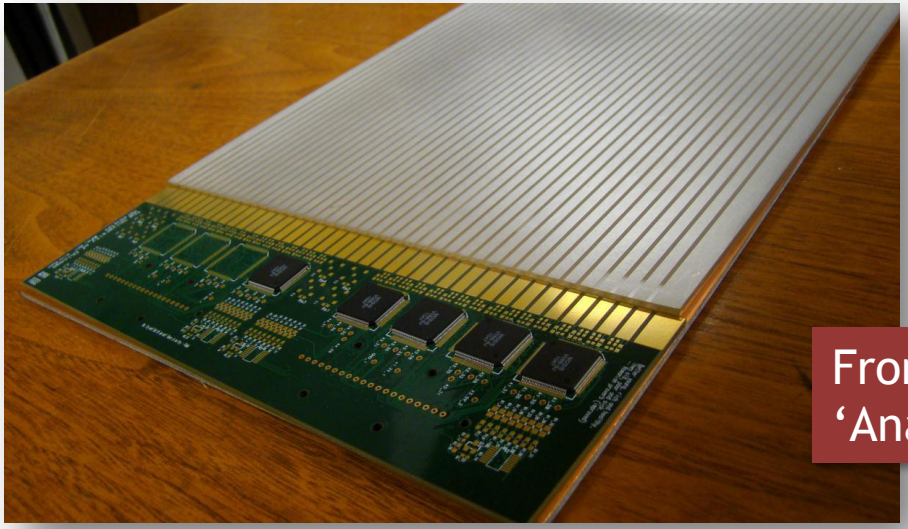
- Location of event (x,y) determined by the time difference of signal on two ends (x) and the charge-centroid of adjacent strips (y)
  - Position resolution <--> time resolution **[$\sigma_x = \sigma_t * v_{prop}$]**

100 ps ~ 1.5 cm
10 ps ~1.5 mm
…etc.

Front-end Readout

- Custom waveform sampling ASICs readout both ends of microstrip lines
  - → High channel density
  - → Compact electronics integration with detector
  - → Low power
  - → Low cost per channel
  - → Preserve timing information

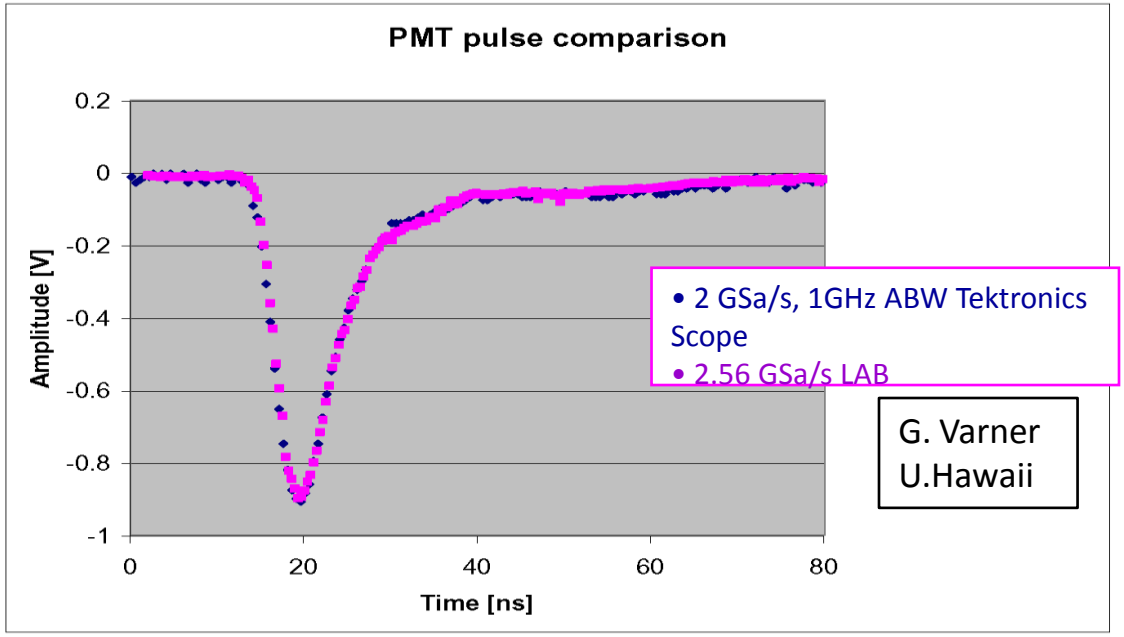




Front-end ASIC 'Analog Card'

Genat, et al.
NIM A**607 (2009) 387-393**.

Waveform Sampling (WFS) ASICs



WFS ASICS = "analog down conversion" (GHz sampling→ 10-100 MHz readout)

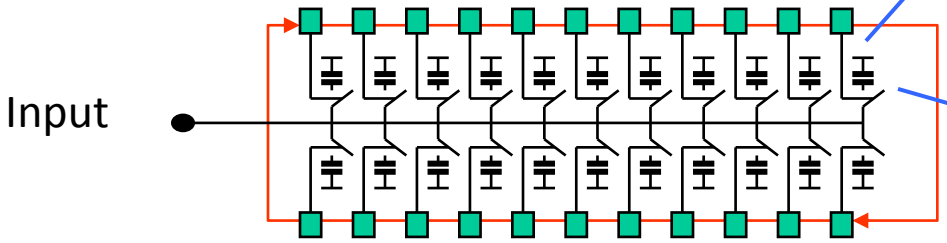
-full waveform reduces impact of noise/poorly formed pulses

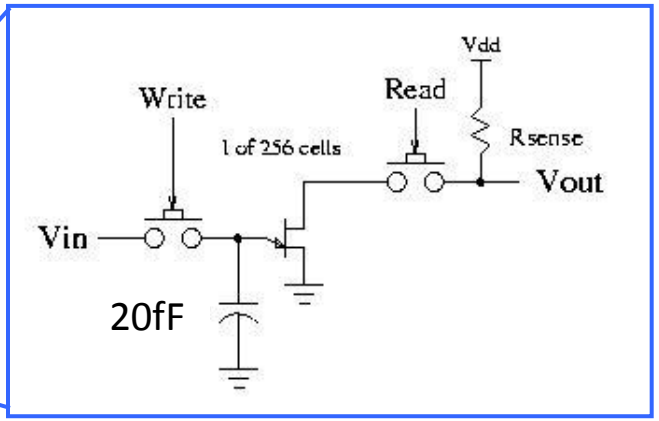
-data processing options

→Useful for most "triggered" 'event' applications

Switched Capacitor Array Sampling

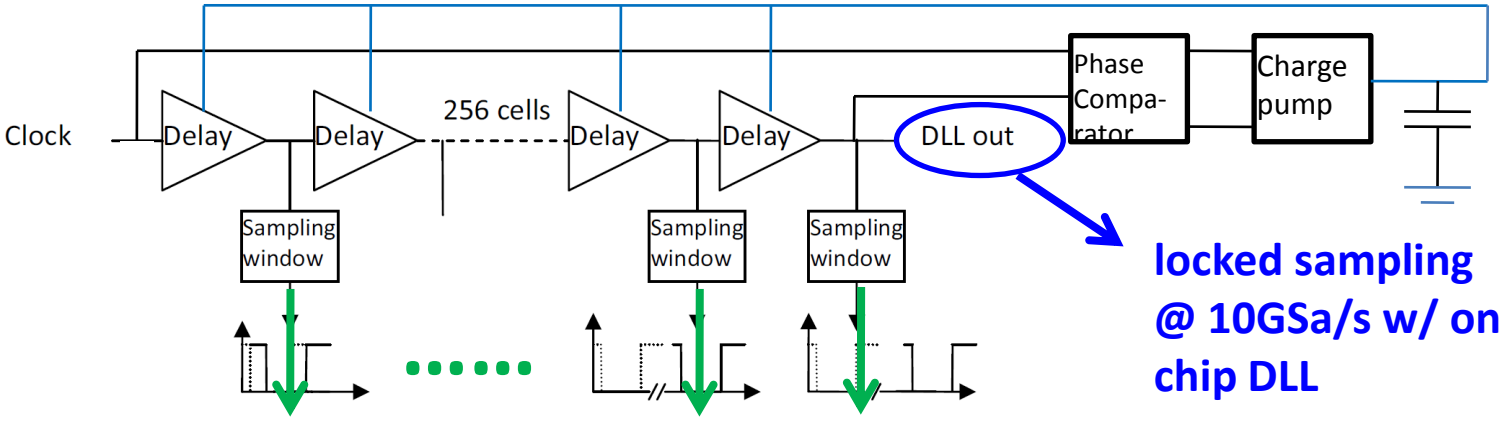
Write pointer passed along array - generates 'sampling window' (~5-10 switches closed at once):





Tiny charge: 1mV ~ 100e$^-$

Timing generation with a delay locked loop (DLL):

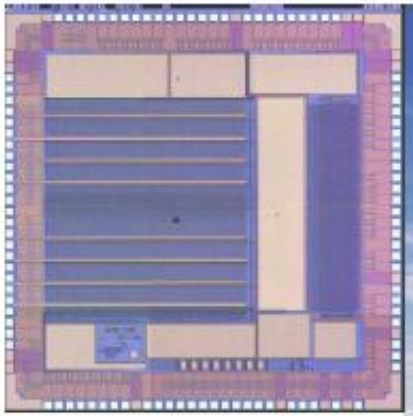


locked sampling @ 10GSa/s w/ on chip DLL

To switched capacitor array – sample & hold

Waveform Sampling ASICs

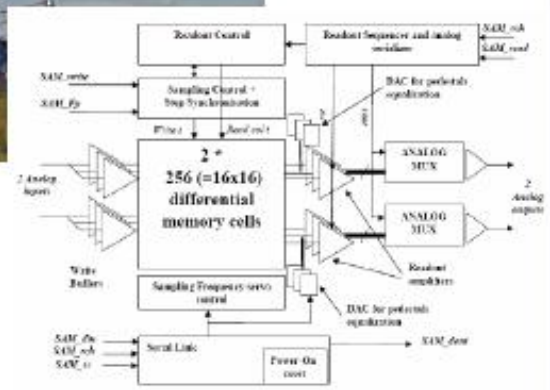
- Already in use in many experiments…

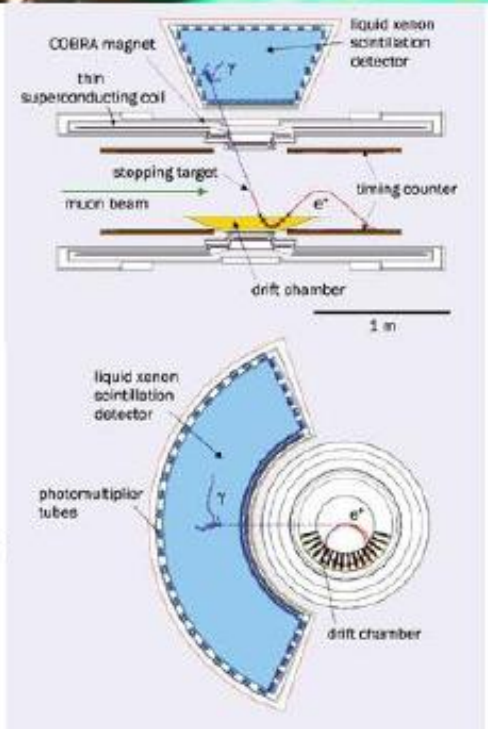


LABRADOR3,
ANITA Experiment

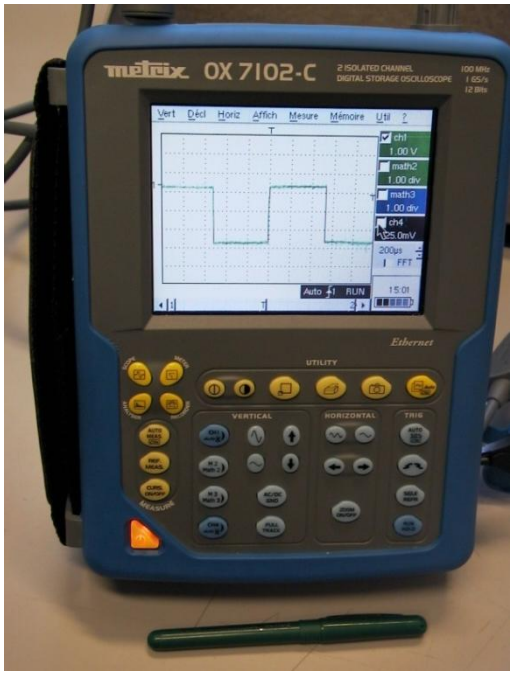
DRS4,
MEG Experiment

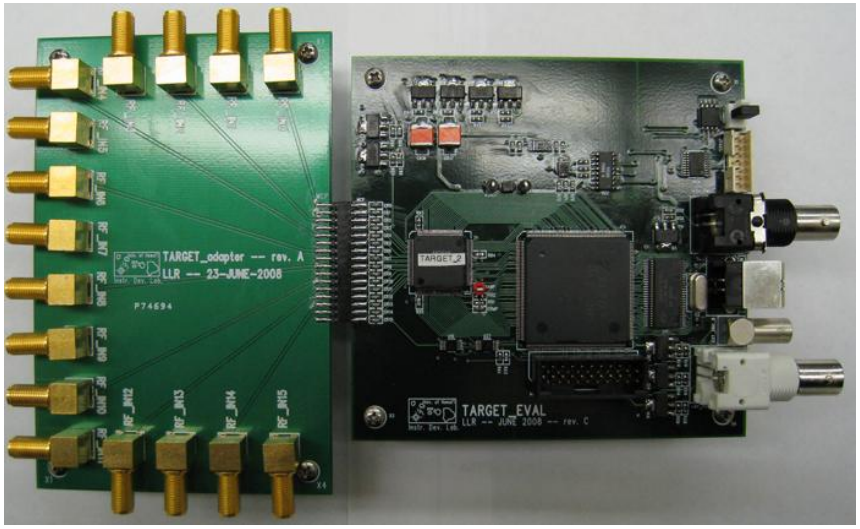
SAM,
H.E.S.S.-II





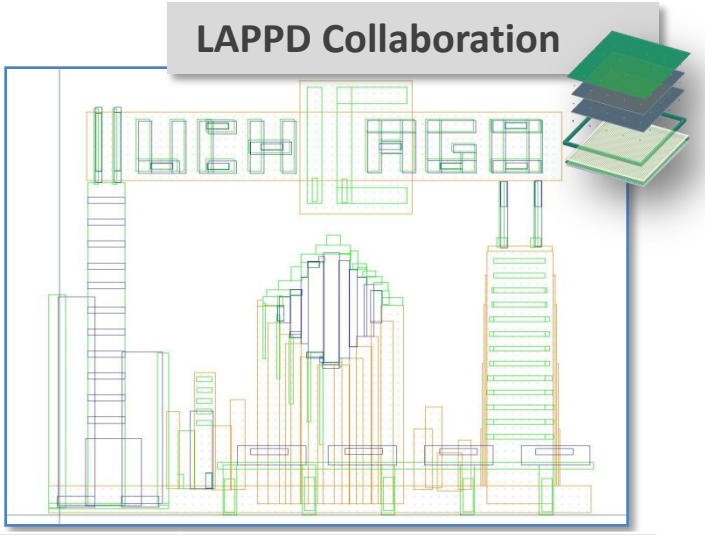
Easy access to Waveform sampling





	WFS ASIC	Commercial
Sampling speed	0.1-15 GSa/s	3 GSa/s
Bits/ENOBs	16/9-13+	8/7.4
Power/Chan.	<= 0.05W	Few W
Cost/Chan.	**~$10s (vol)**	**> > $100**

PSEC-4 ASIC



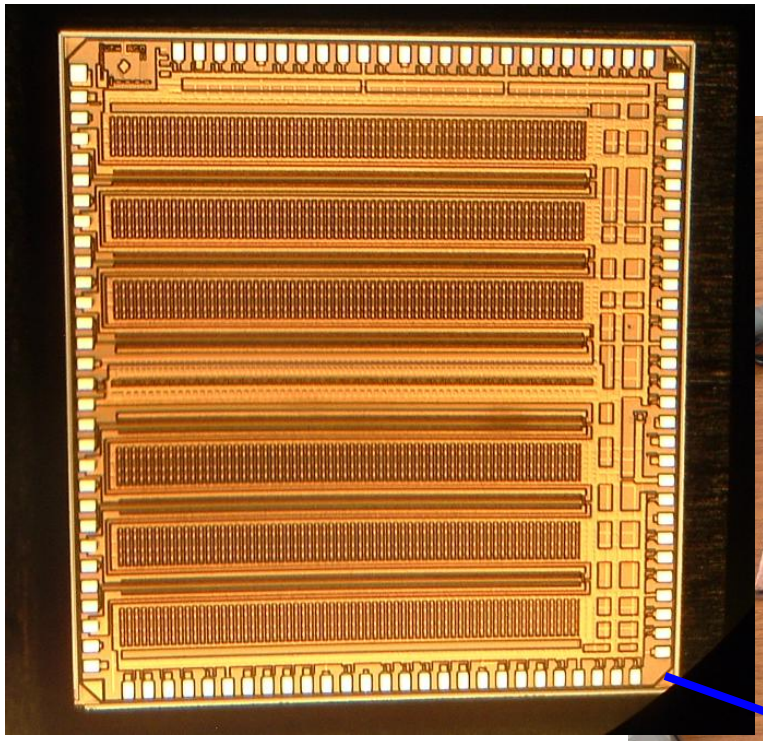
Designed to sample & digitize fast pulses (MCPs):

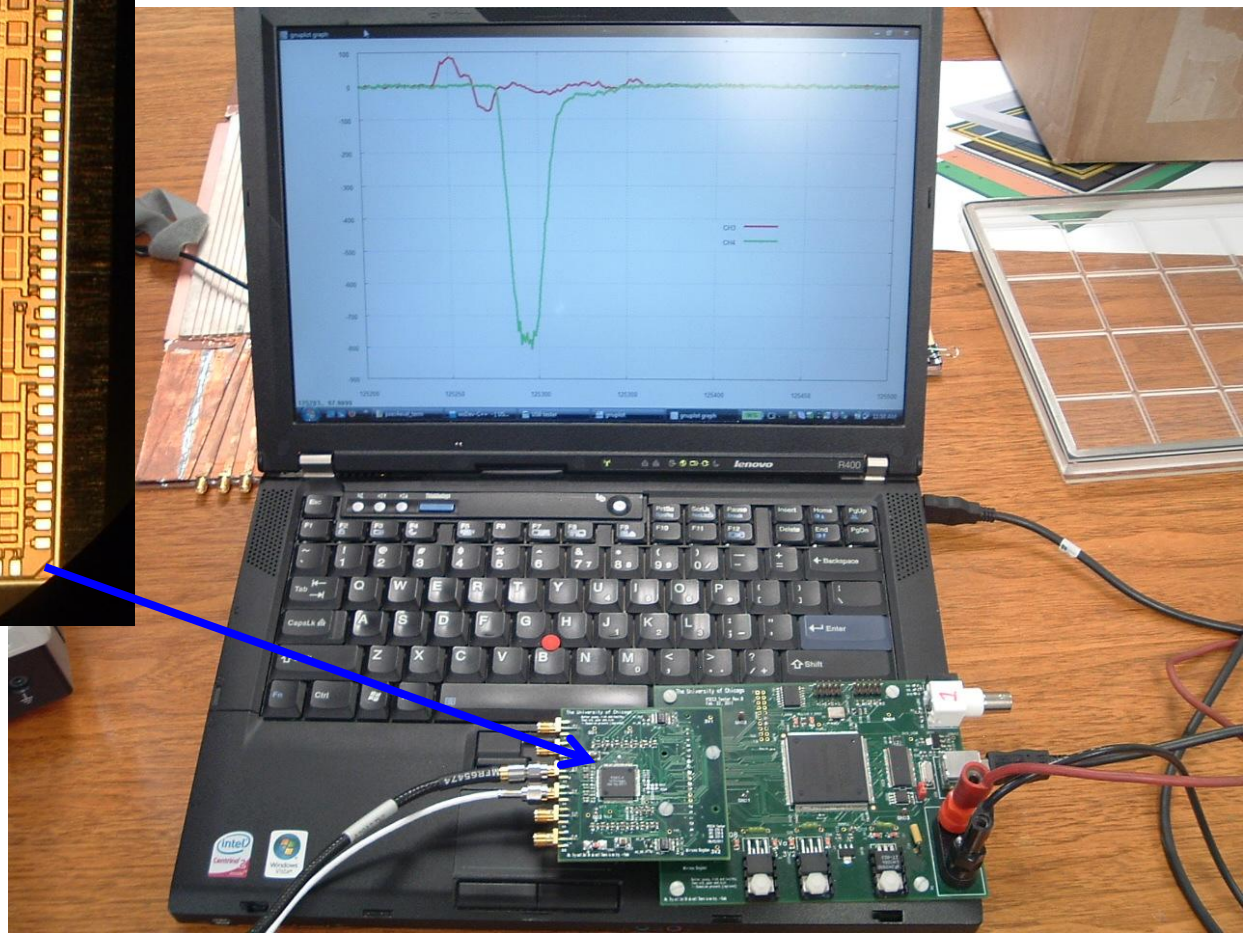
- Sampling rate capability > 10GSa/s
- Analog bandwidth > 1 GHz (challenge!)
- Relatively short buffer size
- Medium event-rate capability (up to 100 KHz)

→ ***130 nm CMOS***

	SPECIFICATION
Sampling Rate	2.5-15 GSa/s
# Channels	6 (or 2)
Sampling Depth	256 (or 768) points
Sampling Window	Depth*(Sampling Rate)$^{-1}$
Input Noise	<1 mV RMS
Analog Bandwidth	1.5 GHz
ADC conversion	Up to 12 bit @ 2GHz
Dynamic Range	0.1-1.1 V
Latency	2 µs (min) – 16 µs (max)
Internal Trigger	yes

PSEC-4 ASIC

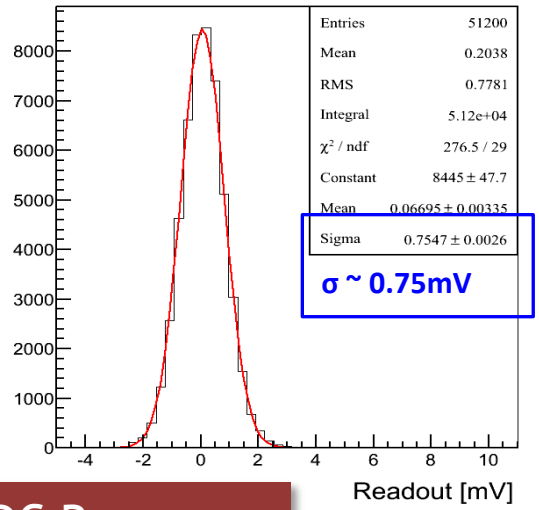




- 6-channel **“oscilloscope on a chip”** (1.6 GHz,10-15 GS/s)
- Evaluation board uses USB 2.0 interface + PC data acquisition software

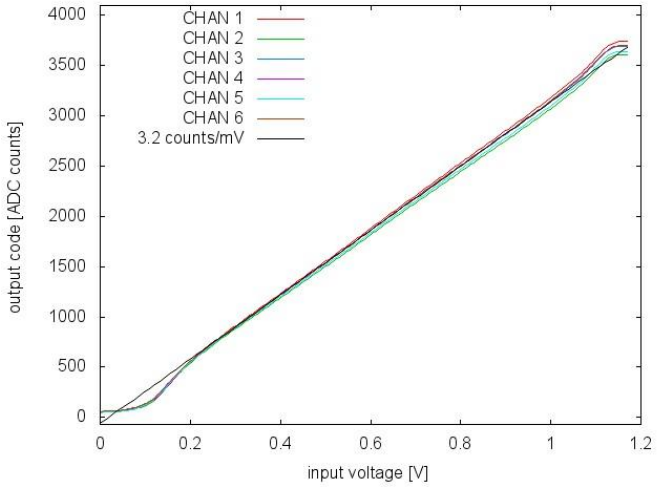
PSEC-4 Performance

Noise

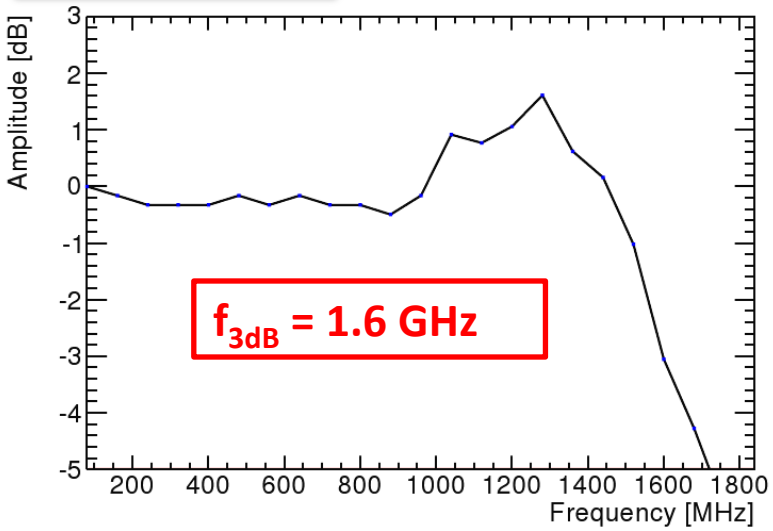


- **Low noise <1 mV**
- **~1V dynamic range with excellent linearity**
- **Analog bandwidth of 1.6 GHz**
- **Sampling rates up to 15 GSa/s**

DC Response



Frequency Response

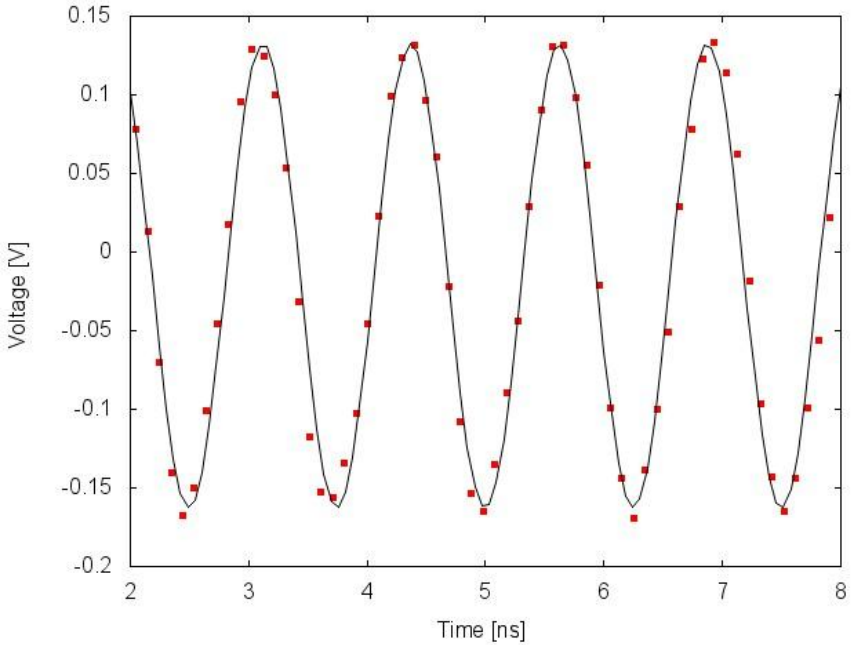


PSEC-4 Performance

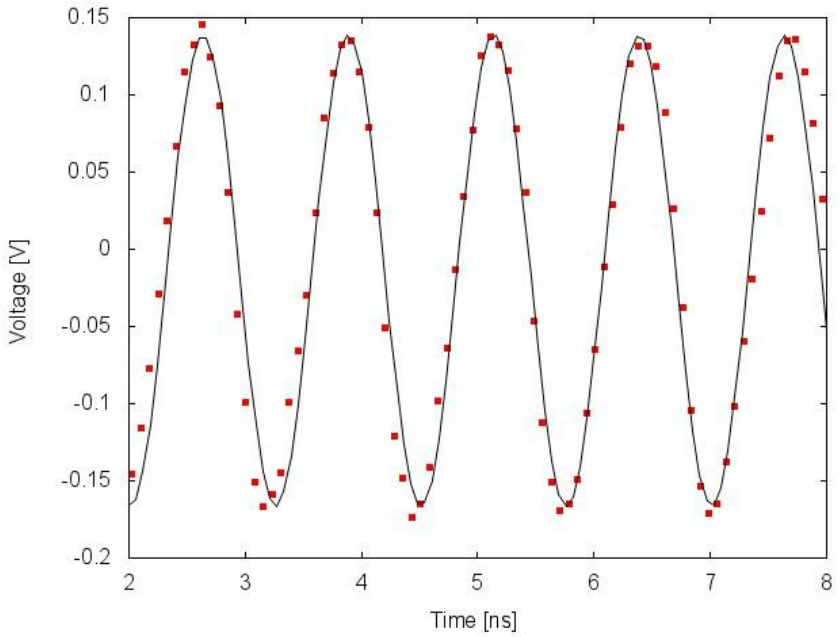
Digitized Waveforms

Input: 800MHz, 300 mV_{pp} sine

Sampling rate : 10 GSa/s



Sampling rate : 13.3 GSa/s



- Only simple pedestal correction to data
- As the sampling rate-to-input frequency ratio decreases, the need for time-base calibration becomes more apparent (depending on necessary timing resolution)

Additional ASIC options…

- PSEC-4 intended for fast sampling & precision timing:
  - recording window of 25-50 ns (256 points per waveform)
- Some applications may require deeper record lengths and/or more complicated triggers – **alternative waveform digitizing ASICs:**

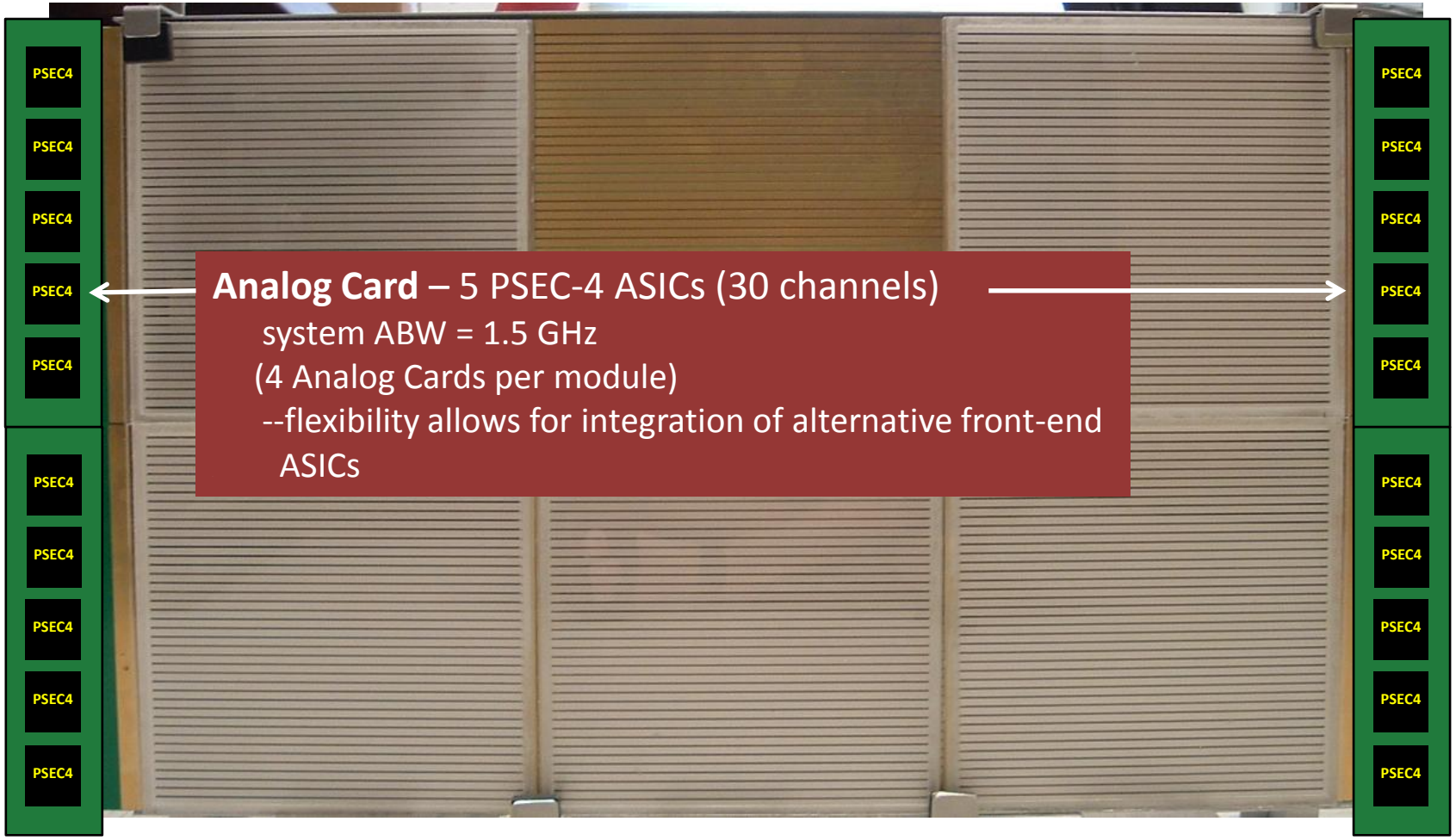
Ice Radio Sampler (IRS) / Buffered LABRADOR 3 (BLAB3) Specifications

32768	samples/chan (8-32us trig latency)
8	channels/IRS ASIC
8	Trigger channels
~9	bits resolution (12-bits logging)
64	samples convert window (~16-64ns)
1-4	GSa/s
1	word (RAM) chan, sample readout
16	us to read all samples
100's	Hz sustained readout (multibuffer)

G. Varner
U.Hawaii

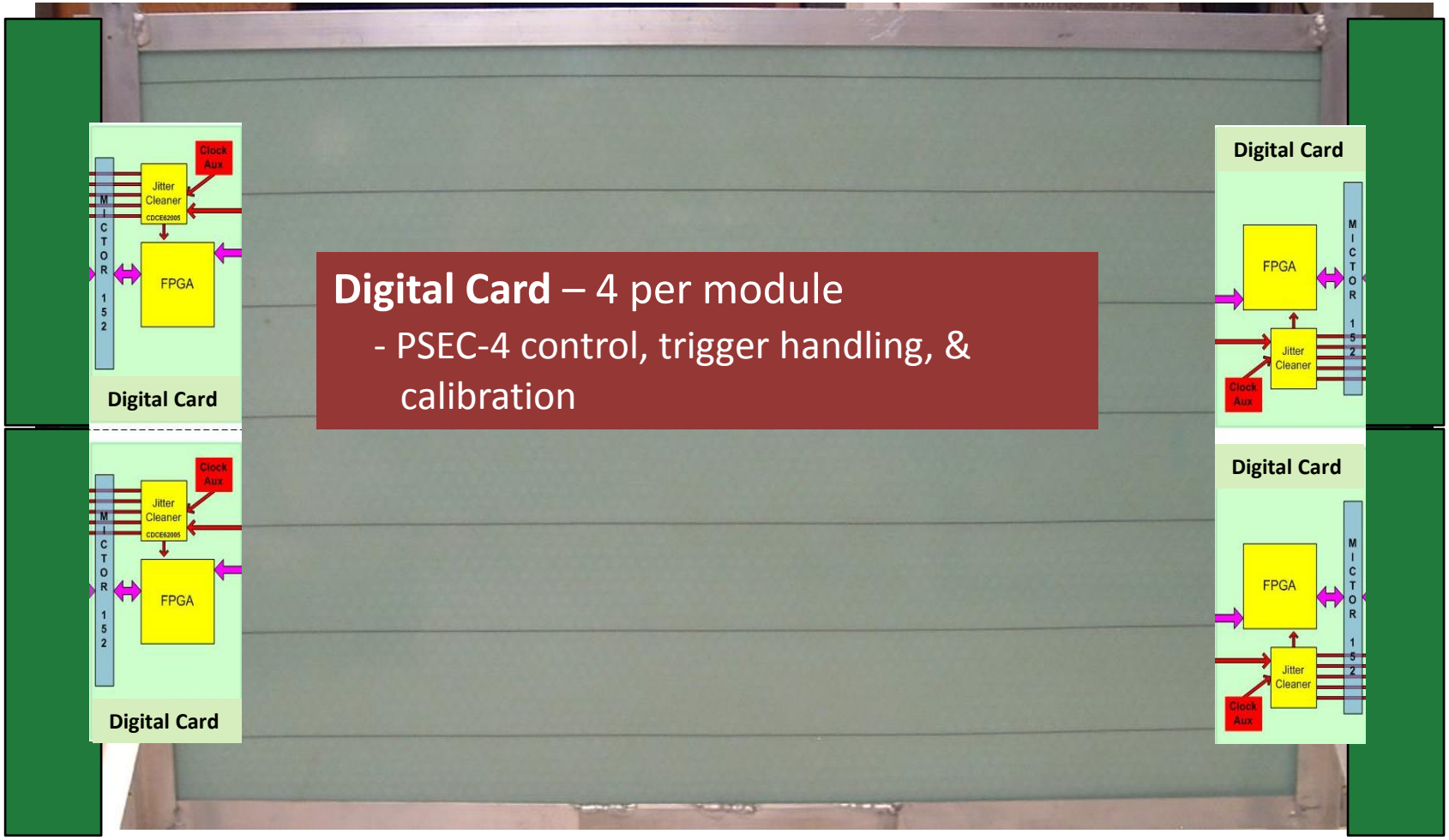
DAQ system

- Targeted to Super Module readout



DAQ system

- Backside of Super Module:



DAQ system

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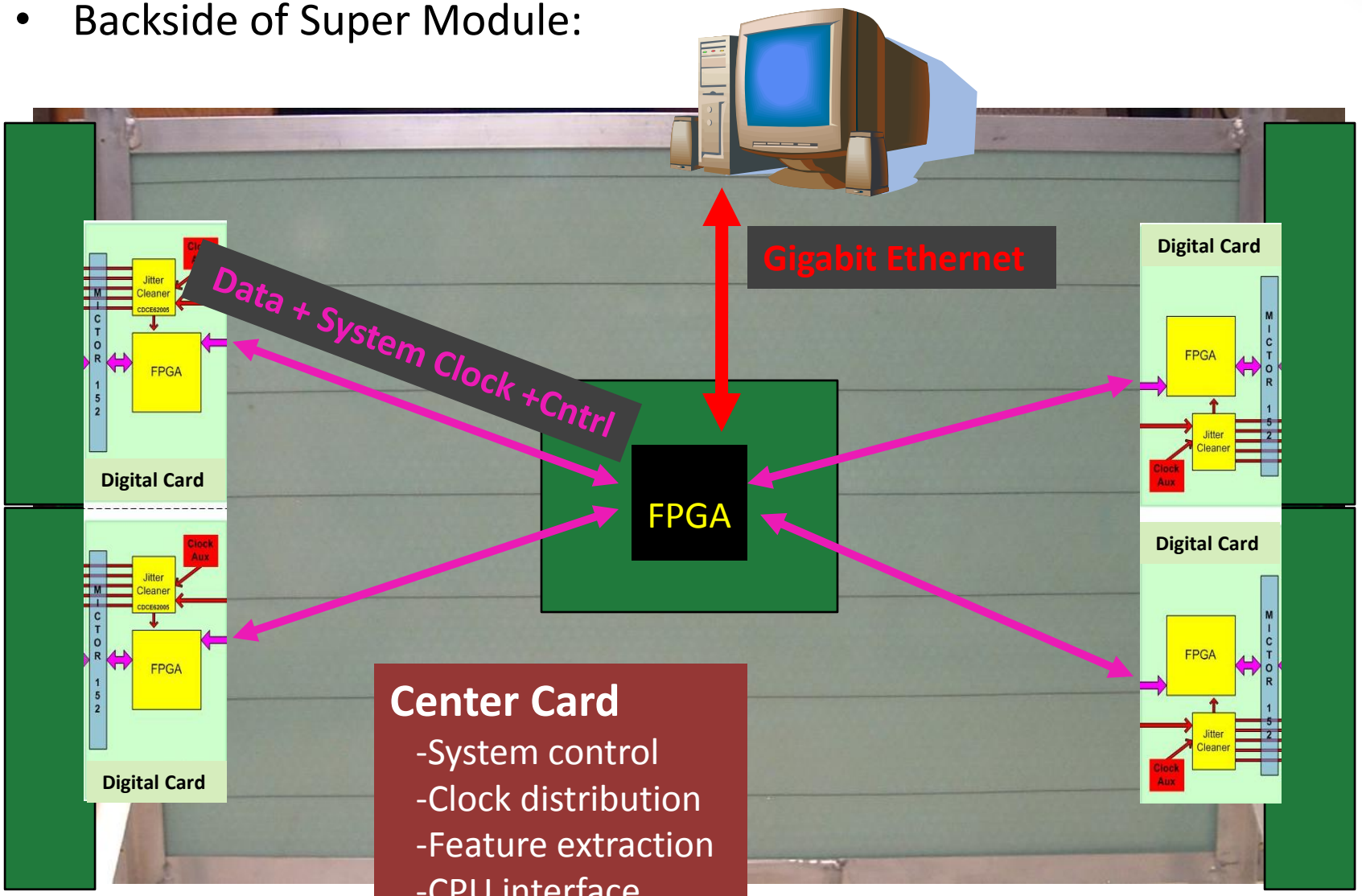
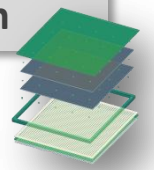
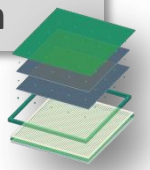




DAQ system

- Design in progress
  - PSEC-4 is baseline WFS ASIC
- Modular – may equip any array of LAPPD 30-microstrip tiles
- Software/firmware development
- System will send event **time, amplitude, goodness of fit, trigger location, etc..** to PC.
  - with option to send entire digitized waveform per event



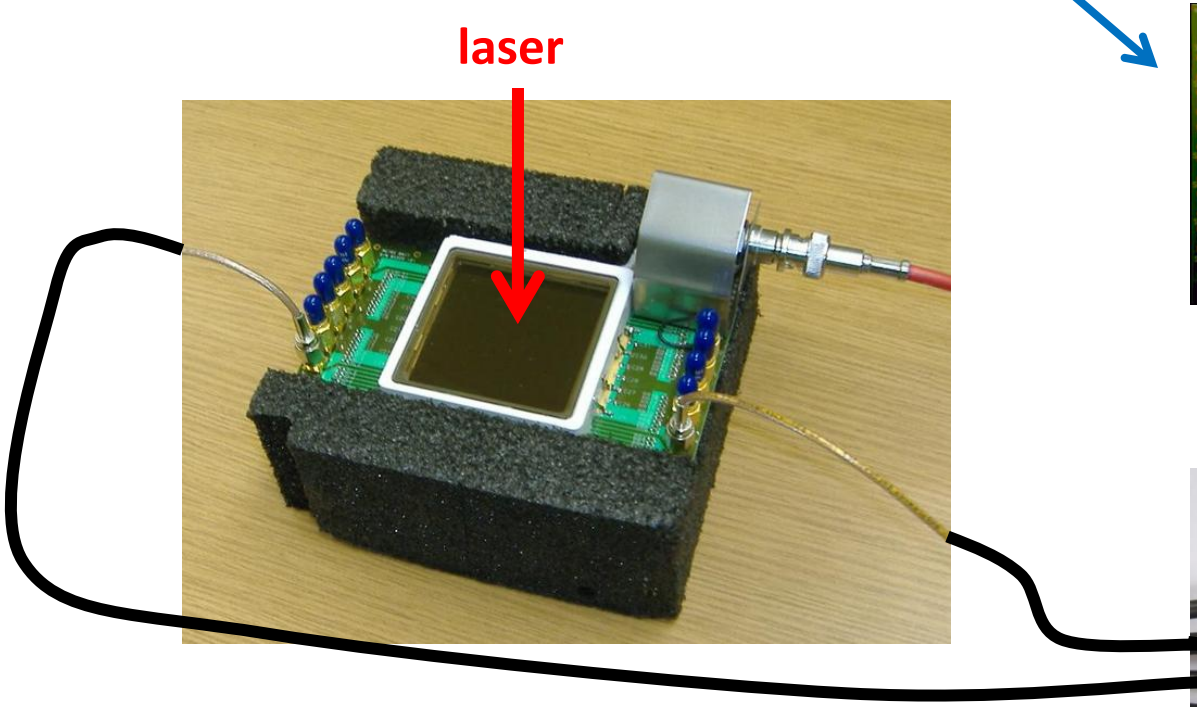
Summary

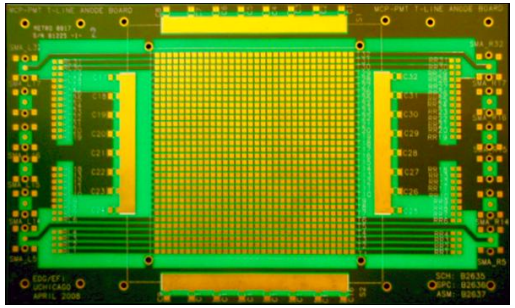
- LAPPD readout using 1.5 GHz transmission line anode
  - Low # of readout channels w/o sacrificing position resolution ($\sigma_t \leq 100$ ps will be achieved → ≤1 cm)
- Front-end readout using waveform sampling ASICs
  - PSEC-4 baseline ASIC (>10GS/s) with deeper sampling options available--pipelined operation
  - Keeping full waveform= potential for better reconstruction?
- DAQ system will be online in a few months
  - w/ functional 8” MCP → beam test will be priority.

backup

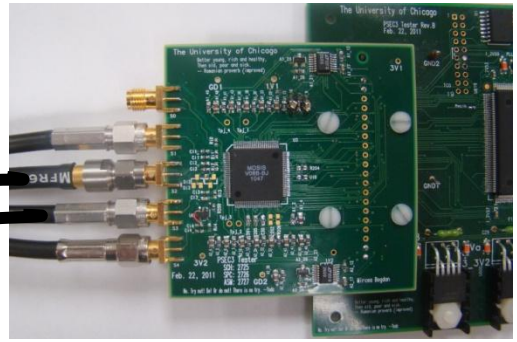
Transmission Line-MCP readout with PSEC-3

2” x 2” Burle Planacon w/ custom PCB T-Line board





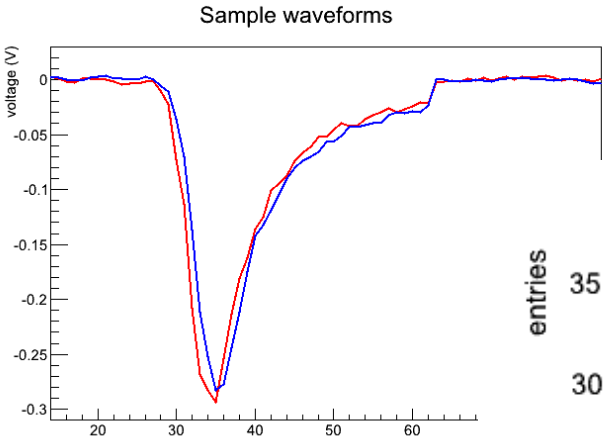
F. Tang - UChicago

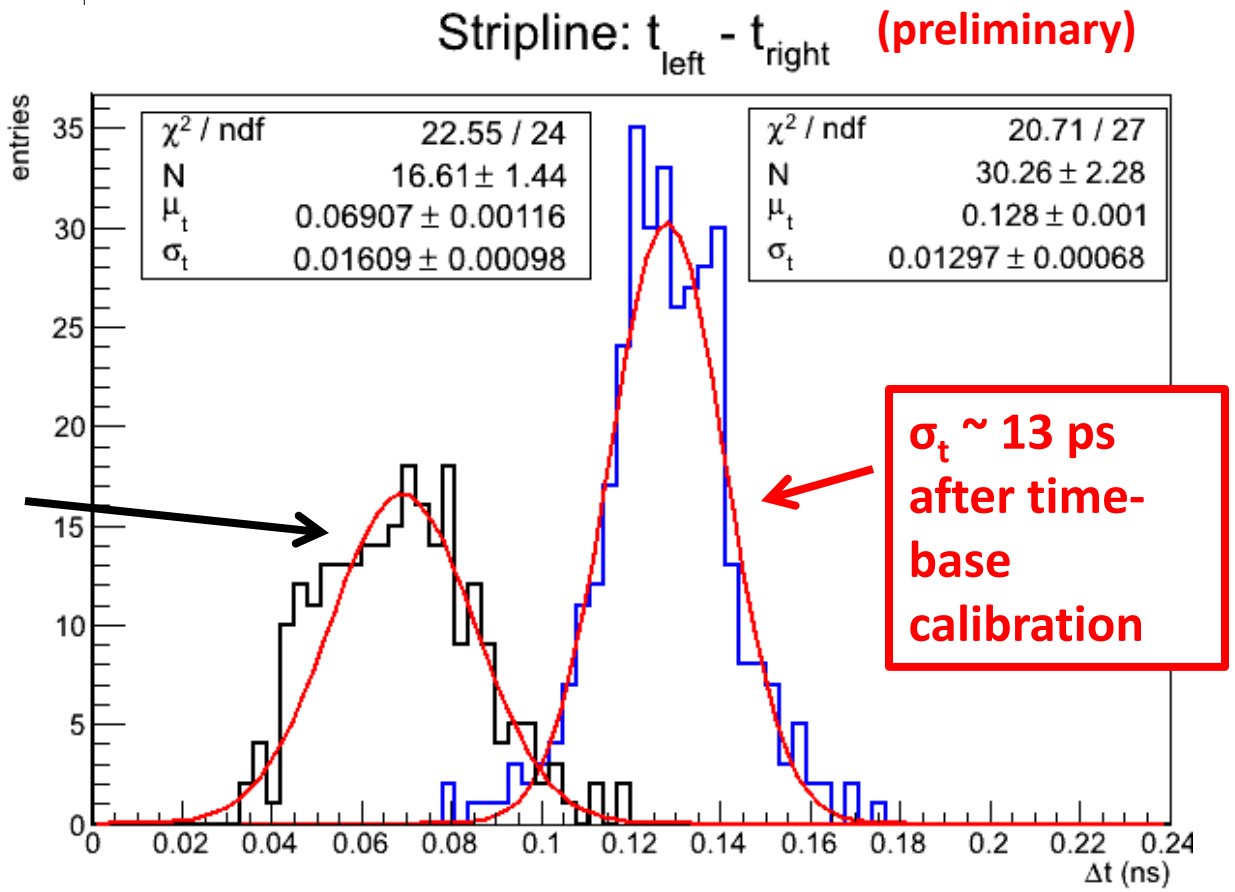


PSEC-3 sampling @ 10 Gsa/s

Transmission Line-MCP readout with PSEC-3

LAPPD Collaboration





σ_t ~ 17 ps assuming nominal 100ps per cell

σ_t ~ 13 ps after time-base calibration

Wilkinson ADC – easy to integrate on-chip